WHAT IS CLAIMED IS:

1. A device for controlling a system time clock (STC) signal of an MPEG decoder comprising:

a first subtractor receiving a plurality of program clock reference (PCR) values and a plurality of STC values, and outputting first gap values being a difference between a respectively received PCR and STC values;

a controller determining whether a current PCR value has been updated two or more times;

a plurality of difference (DIF) registers storing successively output first gap values of the first subtractor if the current PCR value has not been updated two or more times under the control of the controller;

a second subtractor calculating a second gap value being a difference between a current output value of the first subtractor and the first gap value previously stored in the plurality of DIF registers if the PCR value has been updated two or more times, and storing successively calculated second gap values in a plurality of gap registers;

a mean calculator calculating a mean value of the second gap values stored in the gap registers and outputting an output value;

an LPF/gain controller processing the output value from the mean calculator by performing low pass filtering and gain control;

a voltage controlled oscillator outputting a clock signal having a desired frequency by receiving a value from the LPF/gain controller; and

a temporary STC counter counting based on the clock signal, to output the STC value to the first subtractor.

2. The device of claim 1, wherein the output value of the mean calculator is input to the LPF/gain controller through a pulse width modulator (PWM) controller.

3. The device of claim 1, wherein the controller controls the temporary STC counter, the first subtractor, the second subtractor, and the mean calculator, and receives an external PCR extracted value.

4. The device of claim 1, wherein the DIF registers, the gap registers, the temporary STC counter are reset before the first gap values between the plurality of PCR values and the STC value are calculated.

5. A method for controlling a system time clock (STC) of an MPEG decoder comprising the steps of:

increasing a temporary STC value to a desired frequency through an initial reset step;

detecting the presence of a program clock reference (PCR) value in a digital data stream to load the detected PCR value as the temporary STC value;

first calculating a difference between each subsequently detected PCR value and the loaded temporary STC value to obtain first resultant values;

first determining whether a currently detected PCR value has been updated two or more times;

storing the first resultant values when the first determination result indicates the currently detected PCR values have not been updated two or more times and returning to the detecting step;

second calculating gap values between a current first resultant value and the stored first resultant values to obtain second resultant values;

updating the first resultant values and storing the second resultant values;

second determining whether a predetermined number of the detected PCR values have been updated two or more times;

obtaining a mean value of the stored second resultant values if the second determination result indicates the predetermined number of the detected PCR values have been updated two or more times;

returning to the detecting step of the PCR values if the second determination result indicated the predetermined number of the detected PCR values have not been updated two or more times; and

outputting a controlled clock signal with a desired frequency based on the mean value of the second resultant values.

6. A device for controlling a system time clock (STC), comprising:

a plurality of program clock registers to temporarily store a plurality of program clock reference (PCR) values;

a temporary STC counter to count an STC value based on a control clock signal;

temporary STC registers to temporarily store the plurality of temporary STC values counted by the temporary STC counter;

a micro-controller unit (MCU) to calculate a gap value being a difference between a respectively received PCR values and STC values stored in the temporary STC registers;

a plurality of difference registers (DIF) to temporarily store a plurality of first resultant values generated from the gap value between the PCR and STC values of the MCU;

a plurality of gap registers to temporarily store second resultant values generated by calculating a gap value between a current and previous first resultant value stored in the DIF registers;

a controller to check whether all the PCR values have been updated two or more times;

a pulse width modulator (PWM) controller generating a mean value of a predetermined number of the second based resultant values;

an LPF/gain controller to perform low pass filtering and gain control of output from the PWM controller; and

a voltage controlled oscillator to output the control clock signal based on output of the the LPF/gain controller.

7. The device of claim 6, wherein the DIF registers, the PCR registers, the temporary STC registers, the gap registers, and the temporary STC counter are initiated to increase a value of the temporary STC counter to a desired frequency before temporarily storing the plurality of PCR values.

8. A method for controlling a system time clock (STC) of an MPEG decoder comprising the steps of:

detecting respective program clock register (PCR) values and respectively storing the detected PCR values and a temporary STC value;

implementing an interrupt operation to read out the PCR value and the temporary STC counter value and respectively calculating first resultant values of (PCR value – STC value) and second resultant values of (a current first resultant value - a previous first resultant value);

storing the calculated first resultant values in a corresponding register and storing the second resultant values in a corresponding register;

determining whether a predetermined number of the PCR values have been updated two or more times;

obtaining a mean value of the second resultant values and storing the mean value when the determining step determines that the predetermined number of the PCR values have been updated two or more times;

outputting a controlled clock of a desired frequency using the stored mean value; and

generating the temporary STC value based on the controlled clock.

9. The method of claim 8, wherein the interrupt operation is implemented only one time after the predetermined number of the PCR values have been updated without respectively implementing the interrupt operation for the respective PCR values.

10. The method of claim 9, further comprising the step of returning to the step of detecting the PCR values if the determining step determines that the predetermined number of the PCR values have not been updated two or more times.

11. An apparatus for generating a decoder clock signal, comprising:

a detector detecting a plurality of program clock reference (PCR) values encoded by an encoder clocked using an encoder clock signal;

a processor generating a first initial difference value by calculating a difference between a first detected PCR value and a system time clock (STC) value generated when the first PCR value was detected;

the processor generating a second initial difference value by calculating a difference between a second detected PCR value and a STC value generated when the second PCR value was detected;

the processor generating a composite difference value by calculating a difference between the first initial difference value and the second initial difference value;

an oscillator generating a decoder clock signal based on the composite difference value; and

a counter generating the system time clock values based on the decoder clock signal.

12. The apparatus of claim 11, wherein the processor comprises:

a mean calculator calculating an arithmetic mean of the composite difference values for a predetermined number of PCR values detected by the detector.

13. The apparatus of claim 12, further comprising:

a controller determining whether a current PCR value has been updated two or more times; and

a plurality of difference (DIF) registers storing successively the first initial difference values output from the processor if the current PCR value has not been updated two or more times under the control of the controller; and wherein

the processor calculates the second initial difference values if the PCR value has been updated two or more times, and stores successively calculated second initial difference values in a plurality of gap registers.

14. The apparatus of claim 12, wherein the processor comprises:

a first subtractor generating a first initial difference value by calculating a difference between the first detected PCR value and the STC value generated when the first PCR value was detected, and generating a second initial difference value by calculating the difference between a second detected PCR value and the STC value generated when the second PCR value was detected; and

a second subtractor generating the composite difference value by calculating the difference between the first initial difference value and the second initial difference value.

15. The apparatus of claim 14, wherein the processor further comprises:

a plurality of first registers receiving and storing the first and second initial difference values from the first subtractor; and

a plurality of second registers receiving and storing the composite difference values from the second subtractor.

16. The apparatus of claim 15, wherein the processor further comprises:

a mean calculator calculating a mean of the stored composite difference values;

a pulse width modulation (PWM) controller receiving an output from the mean calculator and outputting a pulse width modulated signal based on the output from the mean calculator; and

a low pass filter (LPF) and gain controller low pass filtering and gain controlling the pulse width modulated signal from the PWM controller and supplying a resulting signal to the oscillator.

17. The apparatus of claim 11, wherein the processor comprises:

a common data line;

a plurality of registers commonly connected to the common data line, and storing a plurality of the first and second initial difference values and storing a plurality of the composite difference values; and

a micro-controller operatively connected with the registers via the common data line, generating the first initial difference value, generating the second initial difference value, generating the composite difference value, and calculating an arithmetic mean of the composite difference values for a predetermined number of the PCR values.

18. The apparatus of claim 17, wherein the processor further comprises:

a pulse width modulation (PWM) controller connected with the common data line, receiving an output from the micro-controller, and outputting a pulse width modulated signal; and

a low pass filter (LPF) and gain controller receiving the pulse width modulated signal from the PWM controller, and outputting a low pass filtered and gain controlled signal to the oscillator.

19. The apparatus of claim 18, further comprising a plurality of temporary STC registers connected with the common data line and storing the count values from the counter prior to processing by the micro-controller.